ABSTRACT OF THE DISCLOSURE

A dynamic random access memory (DRAM) cell layout for arranging deep trenches and active areas and a fabrication method thereof. An active area comprises two vertical transistors, a common bitline contact and two deep trenches. The first vertical transistor is formed on a region where the first deep trench is partially overlapped with the first gate conductive line. The second vertical transistor is formed on a region where the second deep trench is partially overlapped with the second gate conductive line.